FAIRCHILD SEMICONDUCTOR®

July 2009

FAN6753
Highly Integrated Green-Mode PWM Controller

Features

- High-Voltage Startup
- Low Operating Current: 2.7mA
- Adaptive Decreasing PWM Frequency to 22KHz
- Built-in Full-Range Frequency Hopping to Reduce EMI Emission
- Fixed PWM Frequency: 65KHz
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking (LEB)
- Synchronized Slope Compensation
- Internal Auto-Recovery Open-Loop Protection
- GATE Output Maximum Voltage Clamp: 18V
- V_{DD} Under-Voltage Lockout (UVLO)
- V_{DD} Over-Voltage Protection (OVP), Auto Recovery / Latch for Option
- Internal Auto-Recovery Sense Short-Circuit Protection for Option
- Constant Power Limit (Full AC Input Range)
- Internal OTP Sensor with Hysteresis
- Built-in 5ms Soft-Start Function
- Built-in LATCH Pin Pull HIGH (> 5.2V) Latch Function

Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame SMPS

Description

The highly integrated FAN6753 PWM controller provides several features to enhance the performance of flyback converters.

To minimize standby power consumption, a proprietary adaptive green-mode function provides frequency modulation at light-load conditions. To avoid acoustic-noise problems, the minimum PWM frequency is set above 22KHz. This green-mode function enables the power supply to meet international power conservation requirements. With the internal high-voltage startup circuitry, the power loss due to bleeding resistors is also eliminated. To further reduce power consumption, FAN6753 is manufactured using the BiCMOS process, which allows an operating current of only 2.7mA.

FAN6753 integrates a full-range frequency-hopping function internally that helps reduce EMI emission of a power supply with minimum line filters. Its built-in synchronized slope compensation achieves stable peak-current-mode control. The proprietary internal line compensation ensures constant output power limit over a wide AC input voltage range, from $90V_{AC}$ to $264V_{AC}$.

FAN6753 provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety should an open-loop or output short-circuit failure occur. PWM output is disabled until V_{DD} drops below the UVLO lower limit, when the controller starts up again. As long as V_{DD} exceeds ~26V, the internal OVP circuit is triggered.

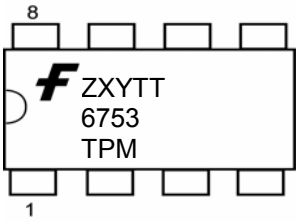
FAN6753 is available in an 8-pin SOP package.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
FAN6753MY	-40°C to +105°C	Green	8-Lead, Small Outline Package	Tape & Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Marking Information



F: Fairchild Logo
Z: Plant Code
X: 1-Digit Year Code
Y: 1-Digit Week Code
TT: 2-Digit Die Run Code
T: Package Type (M:SOP)
P: Y=Green Package
M: Manufacture Flow Code

Figure 1. Top Mark

Pin Configuration

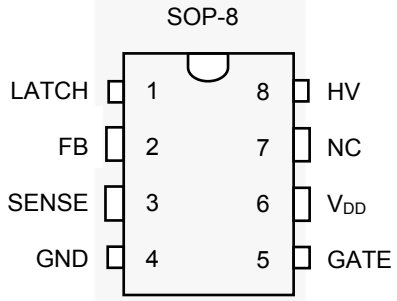


Figure 2. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	LATCH	For external latch circuit used. When $V_{LATCHth}$ > 5.2V and after 100μs, IC is latched off. **10KΩ to GND is recommended. Internal has a sourcing current of 100μA (I_{LATCH}), 100μA ×10KΩ. The voltage on this pin is 1V (under $V_{LATCHth}$=5.2V).**
2	FB	The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal on this pin and the current-sense signal on the SENSE pin.
3	SENSE	Current sense. The sensed voltage is used for peak-current-mode control and cycle-by-cycle current limiting.
4	GND	Ground.
5	GATE	The totem-pole output driver. Soft-driving waveform is implemented for improved EMI.
6	V_{DD}	Power supply. The internal protection circuit disables PWM output as long as V_{DD} exceeds the OVP trigger point.
7	NC	No connection.
8	HV	For startup, this pin is pulled HIGH to the line input or bulk capacitor via resistors.

Application Diagram

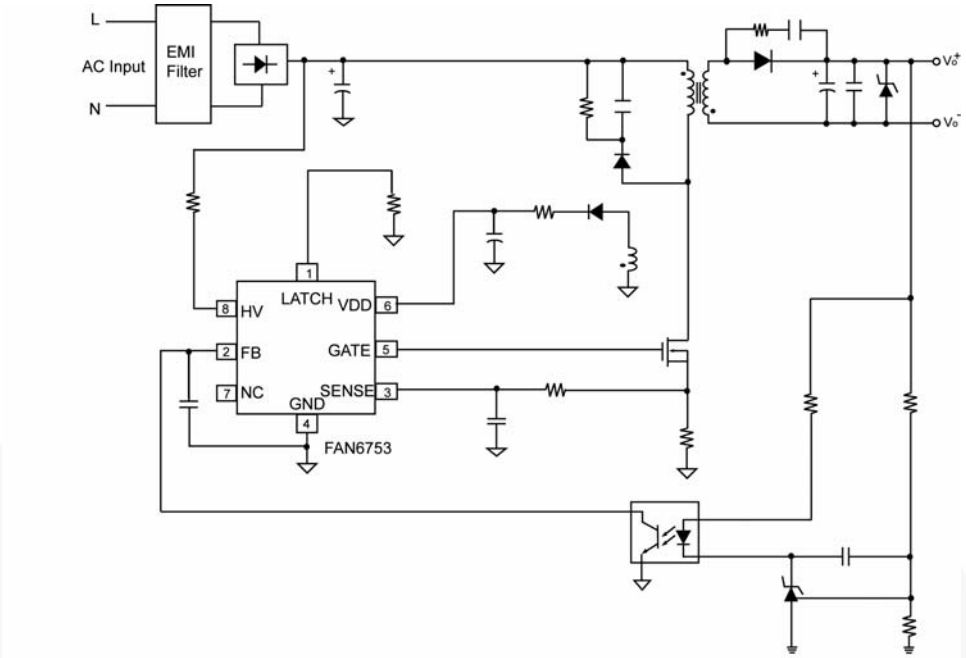


Figure 3. Typical Application

Internal Block Diagram

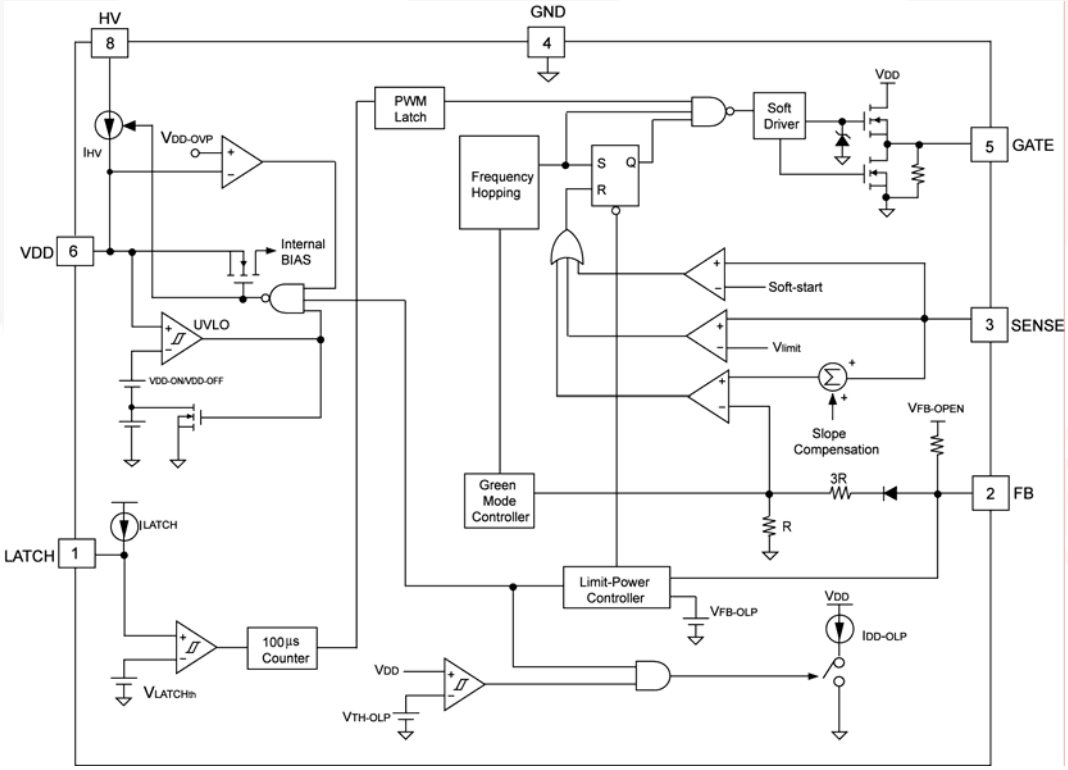


Figure 4. Functional Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	DC Supply Voltage[1, 2]			30	V
V_{FB}	FB Pin Input Voltage		-0.3	7.0	V
V_{SENSE}	SENSE Pin Input Voltage		-0.3	7.0	V
V_{LATCH}	LATCH Pin Input Voltage		-0.3	7.0	V
V_{HV}	HV Pin Input Voltage			500	V
P_D	Power Dissipation ($T_A < 50°C$)			400	mW
Θ_{JA}	Thermal Resistance (Junction-to-Air)			141	°C/W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JEDEC:JESD22-A114		5.5	kV
		Charged Device Model, JEDEC:JESD22-C101		1500	V

Notes:
1. All voltage values, except differential voltages, are given with respect to the network ground terminal.
2. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device

Electrical Characteristics

V_{DD}=15V and T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} Section						
V_{OP}	Continuously Operating Voltage				22	V
V_{DD-ON}	Start Threshold Voltage		14.5	15.5	16.5	V
V_{DD-OFF}	Minimum Operating Voltage		8.5	9.5	10.5	V
I_{DD-ST}	Startup Current	V_{DD-ON} – 0.16V			30	µA
I_{DD-OP}	Operating Supply Current	V_{DD}=15V, GATE Open		2.7	3.7	mA
I_{DD-OLP}	Internal Sink Current	V_{TH-OLP}+0.1V	30	60	90	µA
V_{TH-OLP}	I_{DD-OLP} Off Voltage		6.5	7.5	8.0	V
V_{DD-OVP}	V_{DD} Over-Voltage Protection		25	26	27	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage Protection Debounce Time		75	125	200	µs
HV Section						
I_{HV}	Supply Current Drawn from HV Pin	V_{AC}=90V (V_{DC}=120V), V_{DD}=0V	2.0	3.5	5.0	mA
I_{HV-LC}	Leakage Current after Startup	HV=500V, V_{DD}=V_{DD-OFF}+1V		1	20	µA
Oscillator Section						
f_{OSC}	Frequency in Nominal Mode	Center Frequency	62	65	68	KHz
		Hopping Range	±3.7	±4.2	±4.7	
t_{H-OP}	Hopping Period			4.4		ms
f_{OSC-G}	Green-Mode Frequency		18	22	26	KHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=11V to 22V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A=-20 to 85°C			5	%

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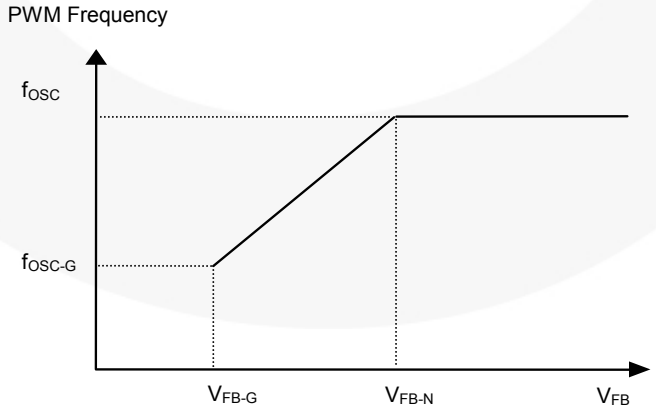

Figure 5. V_{FB} vs. PWM Frequency

Electrical Characteristics (Continued)

V_{DD}=15V and T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
LATCH Section						
$V_{LATCHth}$	Latch-Off Threshold Voltage	$V_{LATCHth}$ > 5.2V, after 100μs Latch Off	5.0	5.3	5.6	V
$t_{D-LATCH}$	Latch-Off De-bounce Time	V_{LATCH}< $V_{LATCHth}$	40	100	160	μs
I_{LATCH}	Output Current from LATCH Pin		92	100	108	μA
Feedback Input Section						
A_V	Input Voltage to Current-Sense Attenuation		1/4.5	1/4.0	1/3.5	V/V
Z_{FB}	Input Impedance		4		7	kΩ
$V_{FB-OPEN}$	Output High Voltage	FB Pin Open	5.0	5.3	5.6	V
V_{FB-OLP}	FB Open-Loop Trigger Level		4.6	4.8	5.0	V
t_{D-OLP}	Delay Time of FB Pin Open-Loop Protection		50	56	62	ms
V_{FB-N}	Green-Mode Entry FB Voltage		2.8	3.0	3.2	V
V_{FB-G}	Green-Mode Ending FB Voltage		2.2	2.4	2.6	V
I_{FB-ZDC}	Zero Duty-Cycle FB Current				1.5	mA
Current-Sense Section						
Z_{SENSE}	Input Impedance			12		KΩ
V_{STHFL}	Current Limit Flatten Threshold Voltage	Duty>40%	0.87	0.90	0.93	V
V_{STHVA}	Current Limit Valley Threshold Voltage	V_{STHFL}–V_{STHVA} Duty=0%	0.30	0.34	0.38	V
t_{PD}	Delay to Output			100	200	ns
t_{LEB}	Leading-Edge Blanking Time		100	140	180	ns
T_{SS}	Period During Soft-Startup Time	Startup Time	4.3	5.0	5.7	ms
GATE Section						
DCY_{MAX}	Maximum Duty Cycle		60	65	70	%
V_{GATE-L}	Gate Low Voltage	V_{DD}=15V, I_O=50mA			1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD}=12V, I_O=50mA	8			V
t_r	Gate Rising Time	V_{DD}=15V, C_L=1nF	150	250	350	ns
t_f	Gate Falling Time	V_{DD}=15V, C_L=1nF	30	50	90	ns
$I_{GATE-SOURCE}$	Gate Source Current	V_{DD}=15V, GATE=6V	250			mA
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=22V			18	V
Over-Temperature Protection Section (OTP)						
T_{OTP}	Protection Junction Temperature[3]			+135		°C
$T_{Restart}$	Restart Junction Temperature[4]			T_{OTP}-25		°C

Notes:
3. When activated, the output is disabled and the latch is turned off.
4. The threshold temperature for enabling the output again and resetting the latch, after over-temperature protection has been activated.

Typical Performance Characteristics

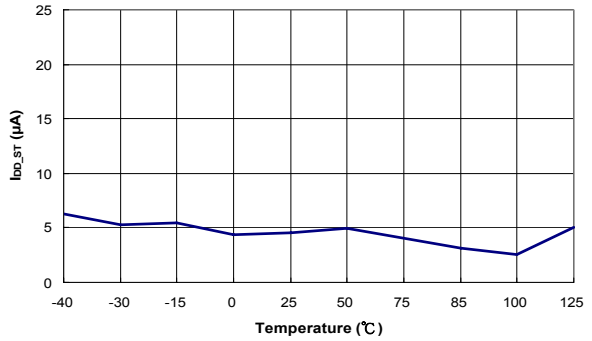

Figure 6. Startup Current (I_{DD-ST}) vs. Temperature

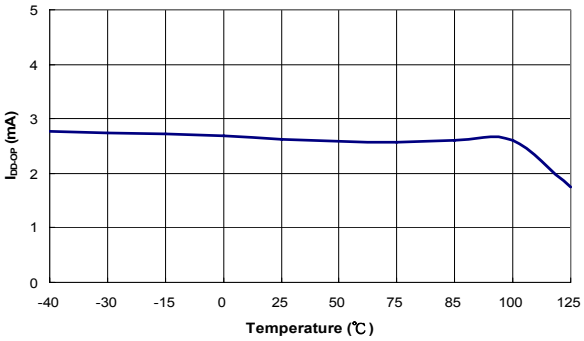

Figure 7. Operation Supply Current (I_{DD-OP}) vs. Temperature

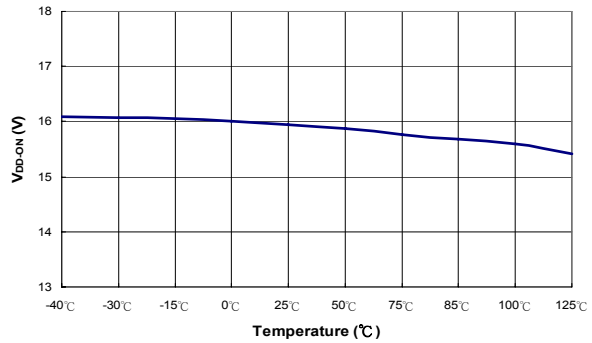

Figure 8. Start Threshold Voltage (V_{DD-ON}) vs. Temperature

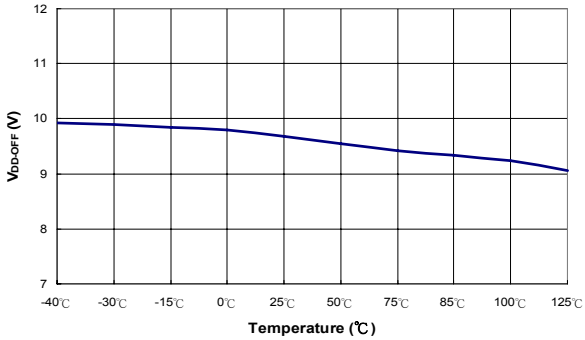

Figure 9. Minimum Operating Voltage (V_{DD-OFF}) vs. Temperature

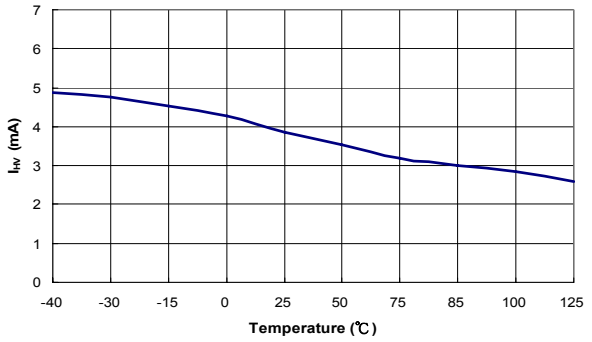

Figure 10. Supply Current Drawn from HV Pin (I_{HV}) vs. Temperature

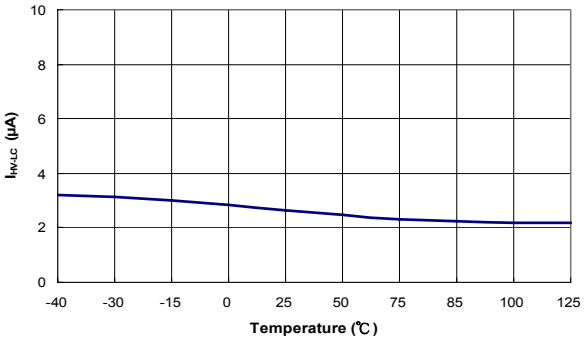

Figure 11. HV Pin Leakage Current After Startup (I_{HV-LC}) vs. Temperature

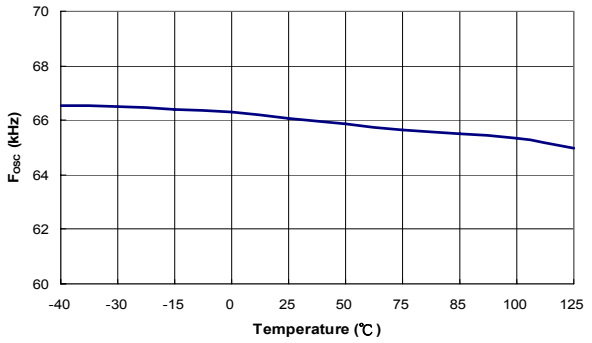

Figure 12. Frequency in Normal Mode (f_{OSC}) vs. Temperature

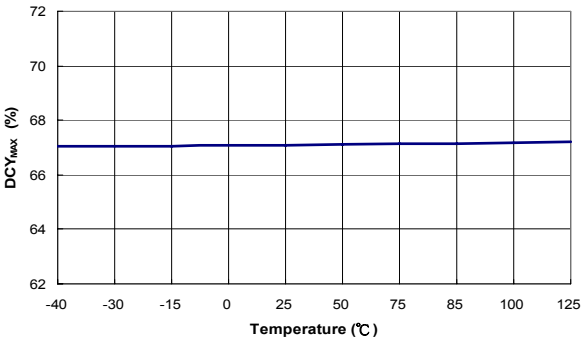

Figure 13. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

Typical Performance Characteristics

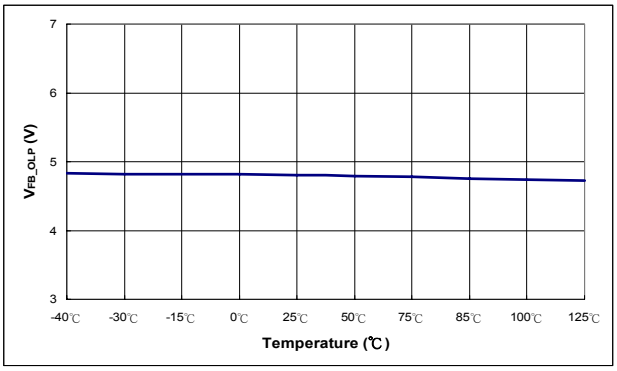

Figure 14. FB Open-Loop Trigger Level (V_{FB-OLP}) vs. Temperature

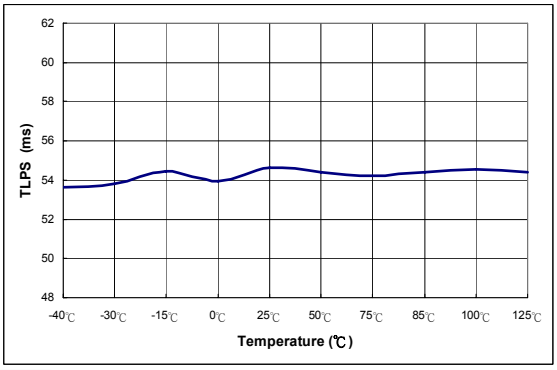

Figure 15. Delay Time of FB Pin Open-Loop Protection (t_{D-OLP}) vs. Temperature

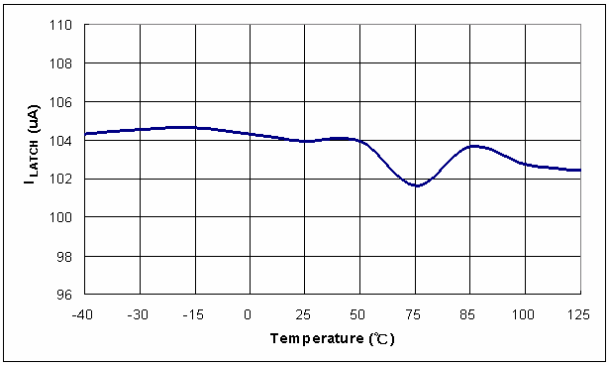

Figure 16. Output Current from LATCH Pin (I_{LATCH}) vs. Temperature

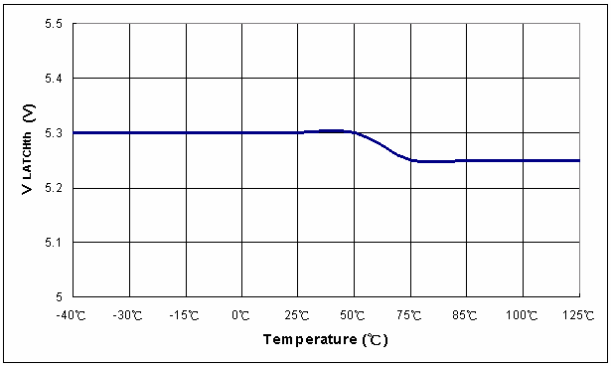

Figure 17. Latch-Off Threshold Voltage ($V_{LATCHth}$) vs. Temperature

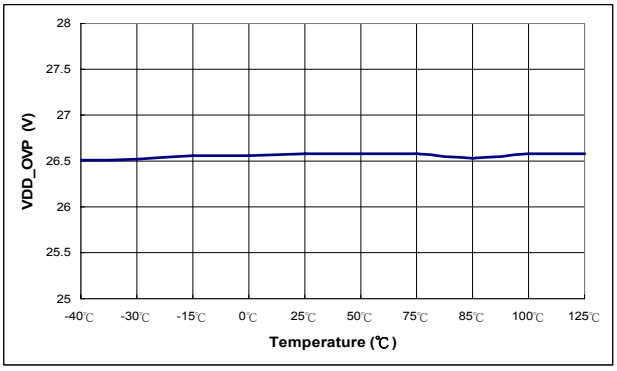

Figure 18. V_{DD} Over-Voltage Protection (V_{DD-OVP}) vs. Temperature

Functional Description

Startup Current

For startup, the HV pin is connected to the line input or bulk capacitor through an external diode and resistor, R_{HV}, (1N4007 / 100KΩ recommended). Typical startup current drawn from the HV pin is 3.5mA and charges the hold-up capacitor through the diode and resistor. When the V_{DD} capacitor level reaches V_{DD-ON}, the startup current switches off. At this moment, the V_{DD} capacitor only supplies the FAN6753 before the auxiliary winding of the main transformer provides the operating current. For higher than 6KV surge test, R_{HV} of 100KΩ or above is recommended.

Operating Current

Operating current is around 2.7mA. The low operating current enables better efficiency and reduces the requirement of V_{DD} hold-up capacitance.

Green-Mode Operation

The proprietary green-mode function provides off-time modulation to reduce the switching frequency in light-load and no-load conditions. The on time is limited for better abnormal or brownout protection. V_{FB}, which is derived from the voltage feedback loop, is taken as the reference. Once V_{FB} is lower than the threshold voltage, the switching frequency is continuously decreased to the minimum green-mode frequency of around 22KHz.

Current Sensing / PWM Current Limiting

Peak-current-mode control is utilized to regulate output voltage and provide pulse-by-pulse current limiting. The switch current is detected by a sense resistor into the SENSE pin. The PWM duty cycle is determined by this current-sense signal and V_{FB}, the feedback voltage. When the voltage on the SENSE pin reaches around $V_{COMP}=(V_{FB}–0.6)/4$, the switch cycle is terminated immediately. V_{COMP} is internally clamped to a variable voltage around 0.9V for output power limit.

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 15.5V and 9.5V, respectively. During startup, the hold-up capacitor must be charged to 15.5V through the startup resistor to enable the IC. The hold-up capacitor continues to supply V_{DD} before the energy can be delivered from auxiliary winding of the main transformer. V_{DD} must not drop below 9.5V during startup. This UVLO hysteresis window ensures that the hold-up capacitor is adequate to supply V_{DD} during startup.

Gate Output / Soft Driving

The BiCMOS output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18V Zener diode to protect power MOSFET transistors against undesirable gate over voltage. A soft driving waveform is implemented to minimize EMI.

Soft-Start

For many applications, it is necessary to minimize the inrush current at startup. The built-in 5ms soft-start circuit significantly reduces the startup current spike and output voltage overshoot.

Built-in Slope Compensation

The sensed voltage across the current-sense resistor is used for peak-current-mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillation. FAN6753 inserts a synchronized, positive-going ramp at every switching cycle.

Constant Output Power Limit

When the SENSE voltage across sense resistor R_S reaches the threshold voltage, around 0.9V, the output GATE drive is turned off after a small delay, t_{PD}. This delay introduces an additional current proportional to $t_{PD} \bullet V_{IN} / L_P$. Since the delay is nearly constant regardless of the input voltage V_{IN}, higher input voltage results in a larger additional current and the output power limit is higher than under low input line voltage. To compensate this variation for a wide AC input range, a sawtooth power-limiter is designed to solve the unequal power-limit problem. The power limiter is designed as a positive ramp signal fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs.

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection is built in to prevent damage due to abnormal conditions. If the V_{DD} voltage is over the over-voltage protection voltage (V_{DD-OVP}) and lasts for $t_{D-VDDOVP}$, the PWM pulses are disabled until the V_{DD} voltage drops below the UVLO, then starts again. Over-voltage conditions are usually caused by open feedback loops.

External Latch Function (LATCH Pin)

The LATCH pin can be used to control the FAN6753 entering latch mode by pulling this pin over 5.2V for 100μs. If floating, the LATCH pin is internally pulled HIGH to 3.5V. It is not recommended to float or short the LATCH pin to GND. This pin also includes a test mode to disable the jitter function. LATCH pin internally sources 100μA, so place a resistor in series to GND. Do not let this voltage exceed 5.2V for the FAN6753 to function normally.

Functional Description (Continued)

Limited Power Control

The feedback (FB) voltage increases every time the output of the power supply is shorted or overloaded. If the FB voltage remains higher than a built-in threshold for longer than $t_{D\text{-}OLP}$, PWM output is turned off. As PWM output is turned off, V_{DD} begins decreasing.

When V_{DD} goes below the turn-off threshold (~9.5V), the controller is totally shut down. V_{DD} is charged up to the turn-on threshold voltage of 15.5V through the startup resistor until PWM output is restarted. This protection feature continues as long as the overloading condition persists.

Over-Temperature Protection (Internal OTP)

The built-in temperature-sensing circuit shuts down PWM output once the junction temperature exceeds 135°C. While PWM output is shut down, V_{DD} gradually drops to the UVLO voltage (around 7.5V). Then V_{DD} charges up to the startup threshold voltage of 15.5V through the startup resistor until PWM output is restarted. This “hiccup” mode protection occurs repeatedly as long as the temperature remains above 130°C. The temperature hysteresis window for the OTP circuit is 25°C.

Noise Immunity

Noise on the current sense or control signal may cause significant pulse-width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FAN6753, and increasing the power MOS gate resistance also improve performance.

Physical Dimensions

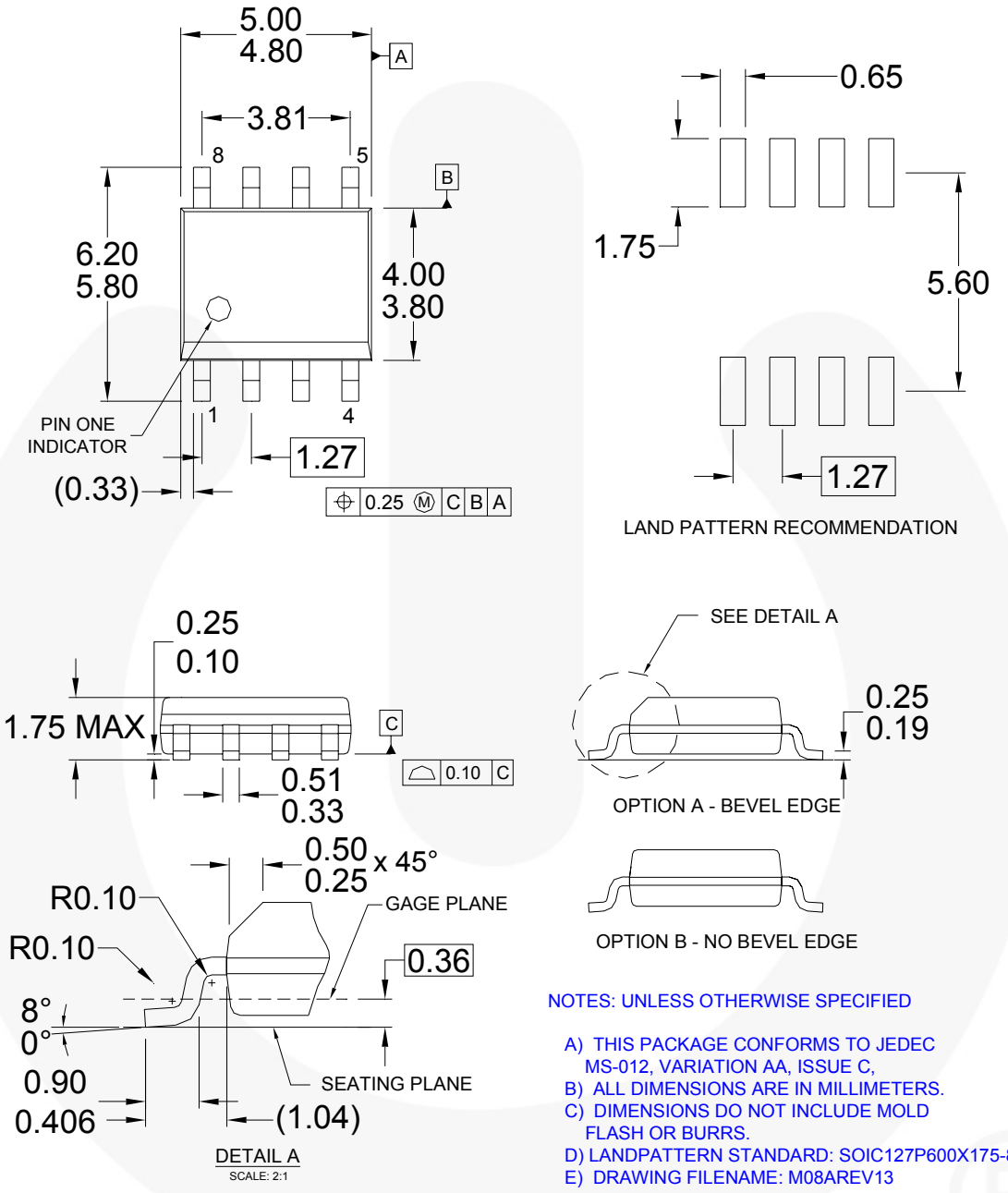

Figure 19. 8-Pin Small Outline Package (SOP)

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FACT®
FAST®
FastvCore™
FETBench™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
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PDP SPM™
Power-SPM™
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
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SMART START™
SPM®
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SuperSOT™-6
SuperSOT™-8
SupreMOS™
SyncFET™
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Definition of Terms

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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